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FAIRCHILD SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation; and ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation, Plaintiffs and Counterdefendants, v. FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation, Defendant and Counterclaimant.	Case No. C 07-2638 JSW (EDL) (Consolidated with Case No. C 07-2664 JSW) **FAIRCHILD SEMICONDUCTOR CORPORATION'S RESPONSIVE CLAIM CONSTRUCTION BRIEF** Date: June 4, 2008 Time: 2:00 p.m. Courtroom: Hon. Jeffrey S. White
AND RELATED COUNTERCLAIMS.	

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I. INTRODUCTION

Fairchild Semiconductor Corporation ("Fairchild") submits this brief in response to the Opening Claim Construction Brief ("Opening Brief") of Alpha & Omega Semiconductor, Ltd., and Alpha & Omega Semiconductor, Inc., (collectively, "AOS") that addressed the three AOS patents asserted against Fairchild: U.S. Patent Nos. 5,767,567 ("the '567 patent"), 5,907,776 ("the '776 patent"), and 5,930,630 ("the '630 patent").[1] AOS claims that its constructions "are faithful to the claimed inventions and comport with the actual patent contribution." AOS's Opening Brief (Docket No. 147), at p. 1. As discussed below, AOS's arguments in support of its claim construction positions are severely flawed by (1) misrepresenting the intrinsic evidence, (2) failing to provide any evidentiary support for what is bare attorney argument, (3) urging constructions that are completely divorced from the context taught in the patents, and (4) making unsupported statements about the technology that are flat out wrong. Fairchild respectfully submits that careful scrutiny of AOS's claim construction positions requires that they be rejected and that Fairchild's proposed constructions be adopted by the Court.

II. THE '567, '776, AND '630 PATENTS

A. The '567 Patent

1. Background of the Technology

The '567 patent is directed toward a device layout for a power MOSFET and a design or method of packaging the device. Declaration of Eric P. Jacobs in Support of Fairchild's Responsive Claim Construction Brief ("Jacobs Resp. Decl."), Ex. 1 ('567 patent), at col. 1, lns. 9-14. Semiconductor devices, such as power MOSFETs, generally are packaged in a protective structure, out of which extend metal contact structures called "leads" that allow the packaged semiconductor device to be connected to an electrical system such as that on a printed circuit board. Declaration of

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[1] Fairchild is asserting six patents against AOS: U.S. Patent Nos. 6,429,481, 6,521,497, 6,710,406, 6,828,195, 7,148,111, and 6,818,947. Fairchild's opening brief addressed the six disputed claim terms in Fairchild's patents, while AOS's opening brief addressed the four disputed claim terms in AOS's patents. This responsive brief addresses the four disputed claim terms in AOS's patents, while AOS will address in its own responsive brief the six disputed claim terms in Fairchild's patents.

Dr. Richard A. Blanchard in Support of Fairchild's Responsive Claim Construction Brief ("Blanchard Resp. Decl."), at ¶ 11. During the packaging process, the power MOSFET is mounted on a metal "die pad," and a number of lead wires are used to connect the die pad to the leads. (*Id.* at ¶ 12.) All of the drawings in the '567 patent show a "vertical" power MOSFET package in which the source contact is on the top surface of the die and the drain contact is on the bottom surface of the die. (*Id.*) As explained in Fairchild's opening claim construction brief, in a vertical device, current flows vertically between the source and the drain, which are located on opposite sides of the semiconductor chip. In a lateral device, the contacts for the source and the drain are located on the top surface. The drawings in the '567 patent show a typical configuration for making electrical connection with the contacts of a vertical device in which all of the leads except one are electrically connected to either the source electrode on the top surface or the drain electrode on the bottom surface of the semiconductor device. The remaining lead is electrically connected to the gate electrode, located on the top surface.

According to the '567 patent, the prior art identified in the '567 patent did not address the effects of the packaging design on the performance characteristics of the device. ('567 patent, col. 1, lns. 33-37.) In particular, the inventors claimed that the on-resistance of the device was not taken into account when forming the lead wires. However, it was well known at the time that the on-resistance of the device is affected by both the number and the arrangement of the lead wires.[2] Increasing the number of lead wires can improve on-resistance, but the number of lead wires is limited by the size of the leads to which they are connected. ('567 patent, col. 4, lns. 18-24; Blanchard Resp. Decl., at ¶ 27.) The '567 patent follows a simple approach purportedly to address the problem by first determining the number of source lead wires needed (which is a function of performance requirements and the number

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[2] Fairchild's expert, Dr. Richard A. Blanchard, explained in his declaration supporting Fairchild's opening claim construction brief that low on-resistance is an important design goal for a power MOSFET. Declaration of Dr. Richard A. Blanchard in Support of Fairchild's Opening Claim Construction Brief (Docket No. 145) ("Blanchard Decl."), at ¶ 21. On-resistance can be affected by many factors, including the thickness of the semiconductor substrate, the doping concentrations for the regions in the device, and the distance between adjacent cells. The '567 patent addresses a component of on-resistance that may be due to the arrangement of the source bonding wires on the top surface of the die.

of source lead wires the leads can physically accommodate). Then, gate runners are arranged on the surface of the device so as to divide the source metal surface into a number of "sub-contact areas." The size of the sub-contact areas, determined by the arrangement of the gate runners on the surface of the device, is then adjusted so that the ratio of the sizes of the sub-contact areas is proportional to the number of lead wires going into each sub-contact area. Claim 7 of the '567, a method claim, is the only claim that AOS has asserted against Fairchild products.

2. "Several" ('567 patent, claim 7)

Fairchild's Proposed Construction	AOS's Proposed Construction
"three or more"	"two or more"

Fairchild's proposed construction is consistent with the claim language, the patent specification, and standard dictionary definitions. AOS's proposed construction is inconsistent with the remaining language of claim 7, as well as the use of the term "several" in the patent specification. *Moreover, in its opening claim construction brief, AOS mischaracterizes – by selectively quoting – the '567 patent specification, which in fact* ***contradicts*** *AOS's proposed construction.* Furthermore, AOS's construction is inconsistent with the most common dictionary definition of the term "several."

a) Fairchild's proposed construction of "several" is consistent with the claim language

Claim 7, the only claim of the '567 patent asserted in this litigation, recites the terms "plurality" and "several." The separate use of each term strongly suggests that the two terms are intended to have a different meaning. In the absence of any evidence to the contrary, a court "must presume that the use of … different terms in the claims connotes different meanings." *Applied Med. Res. Corp. v. U.S. Surgical Corp.*, 448 F.3d 1324, 1333 n.3 (Fed. Cir. 2006) (citation omitted); *see Outside Box Innovations, LLC v. Travel Caddy, Inc.*, No. 07-1253, 2008 WL 145247, at *4 (C.A.Fed. GA Jan. 15, 2008) (different meanings for "flexible [fabric] . . . panel" and "fabric covered . . . panel"). Since "plurality" is generally understood to mean "two or more," the term several must mean "three or more."

This construction is also consistent with the phrase "set of area proportional ratios," which also

appears in claim 7. The commonly understood meaning of the term "ratio" is "the relation between two similar magnitudes with respect to the number of times the first contains the second." (Jacobs Resp. Decl., Ex. 2 (Webster's Encyclopedic Unabridged Dictionary of the English Language (1996).) In other words, a ratio is a comparison of two things. The term "ratios," which is plural, therefore requires at a minimum a comparison of three things (e.g., A compared with B, and A compared with C, represents two ratios). The claim states that the "sub-contact areas" have a "set of area proportional ratios." Therefore, there must be three or more sub-contact areas. If the term "several" were to mean "two or more," as asserted by AOS, then the phrase "set of area proportional ratios" would have to be rewritten as "set of one or more area proportional ratios" to allow for the singular as well as the plural.

b) Fairchild's proposed construction of "several" is consistent with the patent specification

Fairchild's proposed construction is also consistent with the use of the term "several" in the specification of the '567 patent. *The '567 patent uses the term "several"* ***only*** *when referring to items of three or more in quantity.* For example, with regard to the prior art, the patent describes using gate runners to "divide the source contact surface into ***several*** equally divided areas, e.g., 35-1, 35-2, 35-3, 35-4, and 35-5" (**five items**). ('567 patent at col. 1, lns. 43-45.) With regard to the device shown in Figures 2A and 2B, the patent similarly describes gate runners that "divide the source contact 150 into ***several*** source contact areas, e.g., source contact areas 150-1, 150-2, 150-3, and 150-4" (**four items**). ('567 patent at col. 3, lns. 62-65). With regard to an alternate preferred embodiment, the patent discloses disposing gate runners on the source contact area "thus dividing the source contact area into ***several*** sub-contact areas 150-1, 150-2, 150-3, and 150-4 wherein the ***several*** sub-contact areas 150-1 to 150-4 are arranged with different sizes for substantially distributing the lead-wire contact points 170 uniformly over the source contact area 150" (**four items**). ('567 patent at col. 5, lns. 37-44.)

The patent also describes dividing the source contact areas with "***several*** gate runners 140 disposed thereon …." ('567 patent at col. 5, lns. 45-48). The drawings show no fewer than **three** gate runners. Next, the patent discloses configuring the gate runners "for dividing the source contact area 150 into ***several*** sub-contact areas 150-1 to 150-4 (**four items**) with a set of area proportional ratios, e.g., 4:4:4:3, for disposing ***several*** of the lead wires 160 in each of the sub-contact areas 150-1 to 150-

4 according to the set of area proportional ratios, e.g., 4:4:4:3." (**three or four items**) ('567 patent at col. 5, lns. 51-57.) Finally, the patent discloses an embodiment with a modified layout having gate runners disposed on the source contact area with an angular slant, "thus dividing the source contact area into ***several*** sub-contact areas 220-1, 220-2, 220-3, and 220-4 (**four items**) with slant angles for alignment with the lead-wires 230 for connecting to the lead-frames 240." ('567 patent at col. 6, lns. 15-20.)

AOS argues in its brief that the '567 patent uses the terms "plurality" and "several" interchangeably. *AOS's argument misleads the Court by failing to note that these terms are **never** used interchangeably when referring to groups of two.* In those instances where the '567 patent uses the terms "plurality" and "several" to refer to the same structure, the patent always discloses three or more of those things. For example, the patent uses both the terms "plurality" and "several" in referring to the gate runners shown in Figures 2C and 2D. Those figures show at least **three** gate runners, labeled 140. Similarly, the patent uses both "plurality" and "several" to refer to the sub-contact areas shown in Figure 3. That figure shows **four** sub-contact areas, labeled 220-1, 220-2, 220-3, and 220-4.

AOS represents that column 5, lns. 54 to 55 of the '567 patent ("disposing <u>several</u> of the lead wires … in each of the sub-contact areas") refers to Figure 2C which shows two lead wires in the right-most sub-contact area. AOS's Opening Brief, p. 7, lns. 1-13 (emphasis in original). This is a misrepresentation. *By selectively quoting only a portion of the specification, AOS leaves out text that makes clear that this section of the specification is directed only to Figure 2B.* The full sentence from the specification shows that the description refers to **Figure 2B** because the specification refers to an area proportional ratio of **4:4:4:3** and it identifies the lead wires as **feature 160** (which are identified as such in Figure 2B). ('567 patent at col. 5, lns. 45-57.) The area proportional ratios shown in Figures 2C and 2D are 3:3:3:2 and the lead wires in those drawings are not identified as feature 160. (*Id.*) The complete sentence from the patent states:

> This invention also discloses a method to configure a source contact area 150 on a power MOSFET device 100 by dividing said source contact areas 150 with **several** gate runners 140 disposed thereon, the method including steps of: (a) determining a total number of **lead wires 160** for connecting to a lead frame 120 from the source contact area 150 on the MOSFET power device 100; and (b) configuring the gate runners

> 140 for dividing the source contact area 150 into **several** sub-contact areas 150-1 to 150-4 with a set of area proportional ratios, e.g., 4:4:4:3, for disposing **several** of the **lead wires 160** in each of the sub-contact areas 150-1 to 150-4 according to the set of area proportional ratios, e.g., **4:4:4:3**.

'567 patent at col. 5, lns. 45-57 (emphasis added). By carefully omitting portions of the specification that make it clear the language refers to Figure 2B (which shows **three** lead wires in the right-most sub-contact area) and not Figures 2C or 2D (which each show two lead wires in the right-most sub-contact area), AOS wrongly suggests that the term "several" can refer to two or more lead wires. In the above-quoted section of the specification, the word "several" refers to **three** gate runners, **four** sub-contact areas and **three** or more lead wires. Accordingly, AOS's argument that Fairchild's proposed construction is contradicted by the '567 patent specification is simply wrong.

c) Fairchild's proposed construction of "several" is consistent with dictionary definitions

Finally, the common usage of "several" as meaning "three or more" is supported by dictionaries, including those cited by AOS. Webster's Encyclopedic Unabridged Dictionary of the English Language includes a number of definitions of "several," the first one "being more than two but fewer than many in number or kind: *several ways of doing it*." (Jacobs Resp. Decl., Ex. 3.) Merriam-Webster's Collegiate Dictionary, cited by AOS, also includes a number of definitions of "several," one of which is "more than two but fewer than many." (Jacobs Resp. Decl., Ex. 4.) The definition cited by AOS from the Microsoft Encarta College Dictionary is "a grammatical word indicating a small number." (Jacobs Resp. Decl., Ex. 5.) This definition provides no guidance as to whether AOS's or Fairchild's proposed construction is correct. Finally, the definition cited by AOS from the Oxford English Dictionary Online is "In legal use: More than one." (Jacobs Resp. Decl., Ex. 6.) This also provides no guidance, since the terms of a patent are construed according to the understanding of a person of ordinary skill in the art of the pertinent technology, not according to their "legal use," whatever that means. To the extent they provide relevant definitions, the dictionaries cited by both parties support Fairchild's proposed construction of "three or more," which is consistent with the patent disclosure.

3. “configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios” (‘567 patent, claim 7)

Fairchild's Proposed Construction	AOS's Proposed Construction
“arranging the gate runners, after determining the total number of lead wires, to define several sub-contact areas that are not all equal in size and such that the ratio of lead wires to area is the same for each of the sub-contact areas”	“the placement of gate runners divides the source contact area into sub-contact areas, and a set of area proportional ratios are defined by the ratios of the approximate areas of the sub-contact areas”

Fairchild’s construction reflects the teaching of the '567 patent as well as the problem the patent was intended to resolve. AOS's construction attempts to expand the scope of the claims beyond their intended meaning, and ignores the disclosure of the patent.

a) AOS's proposed construction of the "configuring” limitation is inconsistent with the language of claim 7

Claim 7 of the '567 patent is a method claim including two steps. Step (a) involves "determining a total number of lead wires …," and step (b) involves "configuring said gate runners … for disposing ***said*** lead wires in each of said sub-contact areas …." AOS implicitly argues that the steps of the claimed invention need not be performed in accordance with the order in which they appear in the patent claim. AOS's argument, however, is undermined by the use of the term "said" before "lead wires" in step (b). This makes clear that the "lead wires" referred to in step (b) are the same lead wires whose total number was determined previously in step (a). In the context of the claim language, step (b) cannot be performed until that determination is made in step (a), and thus the steps must be performed in the order in which they appear in the claim. *Combined Sys. v. Def. Tech. Corp. of Am.*, 350 F.3d 1207, 1211-12 (Fed. Cir. 2003) (order of steps required when "the method steps implicitly require that they be performed in the order written," *citing Interactive Gift Exp., Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1343 (Fed. Cir. 2001). Therefore, AOS's proposed construction is inconsistent with the plain meaning of claim 7.

b) Fairchild's proposed construction of the "configuring” limitation is consistent with the patent specification

The term “configuring,” as applied to the arrangement of gate runners on a source contact area,

does not have a unique technical meaning to a person of ordinary skill in the art. Blanchard Resp. Decl., at ¶ 26. Therefore, it is necessary to look to the '567 patent specification to determine the meaning of this term. *Toro Co. v. White Conso. Industries, Inc.*, 199 F.3d 1295, 1299-1302 (Fed. Cir. 1999); *Phonometrics, Inc. v. Northern Telecom Inc.*, 133 F.3d 1459, 1466 (Fed. Cir. 1998).

(1) The '567 patent specifically teaches how to perform the "configuring" step

The '567 patent provides a very detailed description of what it means to "configure" the gate runners that are disposed on the surface of the die. ('567 patent at col. 3, ln. 67 to col. 4, ln. 53.) First, the patent states that the number of gate runners (N_{GR}) is determined based upon the device characteristics. ('567 patent at col. 4, lns. 11-14.) For example, larger devices require more gate runners, whereas smaller devices need less gate runners. (*Id.*) The patent teaches that the number of sub-contact areas will necessarily be one more than the number of gate runners (N_{GR}+1). Then, the patent states that the total number of lead wires (N_{LW}) is determined based upon (1) the number of wires the devices needs for the purpose of reducing on-resistance, and (2) the number of lead wires the lead frame can accommodate. ('567 patent at col. 4, lns. 14-24.) Next, the patent teaches determining a basic number of lead wires (N_{BASIC}) and a remainder number of lead wires ($N_{REMAINDER}$) by dividing the number of lead wires by the number of sub-contact areas. ('567 patent at col. 4, lns. 25-35.) The integer portion of the result of the division equals N_{BASIC}, and the remainder of the division equals $N_{REMAINDER}$. (*Id.*) The patent then teaches determining the distribution ratio of the lead wires according to the following rules:

> (1) Each sub-contact area will have either N_{BASIC} or N_{BASIC}+1 lead wires.
>
> (2) The number of sub-contact areas having N_{BASIC}+1 lead wires equals ($N_{REMAINDER}$).
>
> (3) The number of sub-contact areas having N_{BASIC} lead wires equals the total number of sub-contact areas (N_{GR}+1) minus $N_{REMAINDER}$.
>
> (4) The distribution ratio of the lead wires is simply the distribution ratio of lead wires in each of the sub-contact areas.

('567 patent at col. 4, lns. 35-51.) Finally, after all of these steps are completed, the patent teaches dividing the source contact area into sub-contact areas in accordance with the distribution ratio of the

lead wires. ('567 patent at col. 4, lns. 51-53.) *This **final** step corresponds to the "configuring" step of claim 7.* Fairchild's proposed construction is entirely consistent with this teaching in the patent.

(2) The background of the invention requires that the "configuring" step take into account the total number of lead wires

The background section of the patent makes clear that the order in which the steps are performed is critical. The background states that a problem with prior art techniques for designing power MOSFETs was that the design process did not take into account how the device would be packaged. ('567 patent at col. 1, lns. 25-37.) The patent states that the packaging for the device affects its performance characteristics. (*Id.*) Specifically, the patent states that when the device is packaged, lead wires are used to electrically connect the transistor with the pins (i.e., leads) of the package. (*Id.*) The patent also states that the lead wires affect the performance characteristics of the device. (*Id.*) The patent then points out that because power MOSFETs are designed and packaged in separate steps, the affects of the lead wires on the performance characteristics of the device were not taken into account during the design process. (*Id.*) The disclosed invention, however, takes packaging into account during the design of the power MOSFET by considering the total number of lead wires that will be used in the package, as well as the total number of gate runners that will be used in the device. ('567 patent at col. 3, ln. 67 to col. 4, ln. 53.) The number of lead wires and gate runners are then used to calculate how the gate runners will be "configured," i.e., arranged on the source contact area. (*Id.*) If the total number of lead wires were not determined before the configuring step, then the problem identified in the background section of the patent would not be addressed at all.

(3) The disclosed method for performing the "configuring" step will not work if the total number of lead wires are not determined before the gate runners are arranged

The total number of lead wires must be determined before the gate runners are configured. This is because the gate runners are configured based upon the distribution ratio of the lead wires. It would be impossible to determine the distribution ratio of the lead wires without knowing the total number of lead wires. Accordingly, none of the four equations provided in column four of the '567 patent can be performed if the total number of lead wires is not known. In fact, the total number of

lead wires appears in every single equation listed in column four of the '567 patent. Moreover, reversing the order (i.e., configuring the gate runners before determining the total number of lead wires) would frustrate the purpose of the invention, which is to provide the necessary number of lead wires and gate runners to achieve the desired performance. If the gate runners were configured first, before determining the number of lead wires, then the area-proportional ratios (and also the distribution ratio of the lead wires) would be fixed before determining the number of gate runners. Thus, the total number of gate runners would be fixed by the area ratios of the sub-contact area, rather than by the number of gate runners that are actually needed. The entire point of the invention is to have as many lead wires as possible, and arrange the gate runners accordingly to form the sub-contact areas. AOS's proposed construction would thwart this purpose, and therefore must be rejected.

(4) Fairchild's proposed construction properly requires that the sub-contact areas not all be of the same size

The patent specification and its prosecution history further support the requirement that the sub-contact areas must be of *unequal* size. This is expressly stated in the patent: "According to a principle of this invention, in order to reduce the spread resistance, the topology of the gate runner 140 specially arranged [sic] … for dividing the source contact areas 150-1 to 150-4 to source contact areas of ***unequal sizes***." (Col. 3, ln. 67 - col. 4, ln. 5, emphasis added). This statement is specifically made in connection with the embodiment of FIGS. 2A and 2B which reflect the subject matter of claim 7. Such a statement defines the extent of a patented invention. *SciMed Life Sys. v. Advanced Cardiovascular Sys.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001). Furthermore, the method described in column 4 teaches how to arrange the sub-contact areas so as to have unequal sizes. No particular formula is needed to create sub-contact areas having equal sizes. In fact, it was well known in the art prior to the filing of the '567 patent to use sub-contact areas of equal size (as is shown in Figure 1A), and to distribute the source current as evenly as possible.

Moreover, the examiner clearly had the same understanding when he allowed the '567 application. In the first and only Office Action, he stated: "Claims 2-9 [of the application (corresponding to issued claims 1-8)] are considered allowable over the art of record because of the recitation of ***different size subcontact areas,*** angled contact areas and configuring [gate runners] according to a set of proportional ratios." (Jacobs Resp. Decl., Ex. 7, Office Action dated September

17, 1997, emphasis added). The applicants expressly accepted this without dispute in a responsive Amendment, stating: "claims 2-9 are allowed over the art of record because of the specific recitation of ***different size sub-contact areas***, angled contact areas and configurations according to a set of ratios. (Jacobs Resp. Decl., Ex. 8, Amendment dated December 9, 1997, emphasis added). Thus, the examiner viewed the claims as requiring different size sub-contact areas, and applicants' attorney agreed. AOS is now estopped from denying what the applicants accepted. *See Biogen, Inc. v. Berlex Labs., Inc.*, 318 F.3d 1132, 1137-39 (Fed. Cir. 2003) (applicant statements consistent with examiner's reasons for allowance act as disclaimer.) Thus, both the patent specification and its prosecution history clearly support Fairchild's position that the sub-contact areas cannot all be the same size.

c) There is no justification for adding the term "approximate" to the construction of the "configuring" limitation

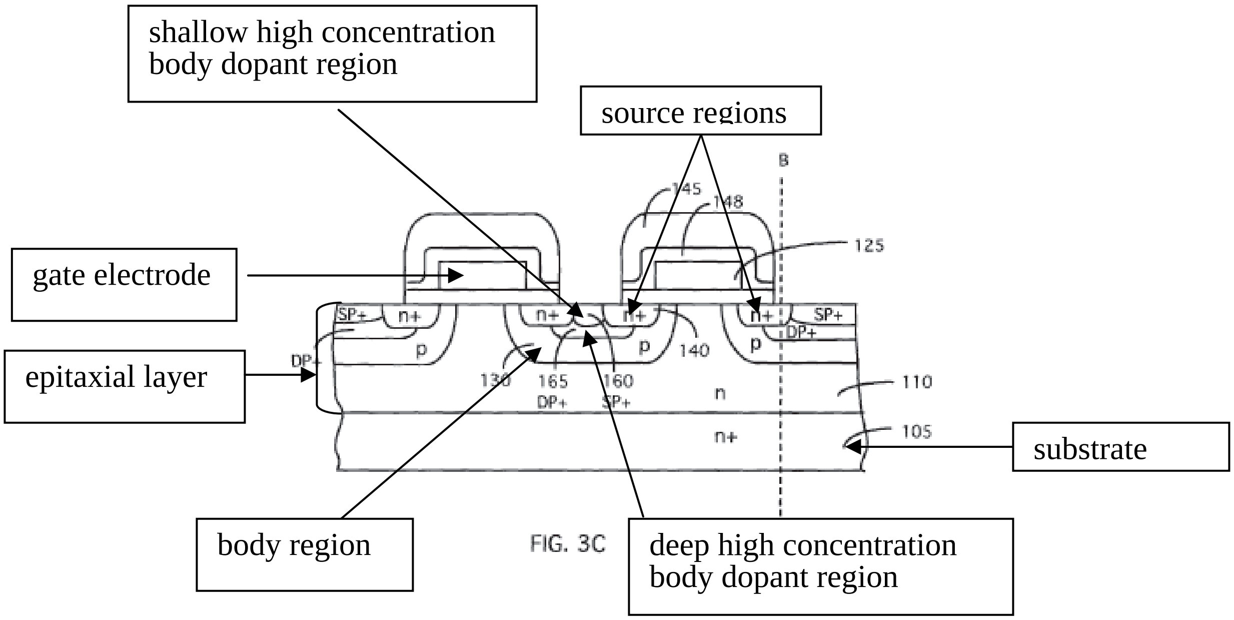
AOS argues that Fairchild has added a limitation by not including the term "approximate" in its proposed construction. In other words, AOS contends that ***by not adding*** a term to the claim language, Fairchild has allegedly ***added*** an extraneous limitation. AOS's argument is nonsense. The claim language never uses the term "approximate." There is nothing in the claim language to suggest that the term "approximate" should be added. While the specification uses the term "approximate" with regard to the area proportional ratios, the inventors chose not to include the term "approximate" in the claim language. The inventors are bound by their choice of words. *See* Kahrl, Patent Claim Construction, § 4.03[E][4] (2001 & 2007 Supp.) ("The patentee is presumed to have intended every word chosen in a claim to have a specific function in adding to the meaning of the claim.") (citation omitted) (Jacobs Resp. Decl., Ex. 9).

B. The '630 Patent

1. Background of the Technology

The '630 patent relates to a method of making power MOSFET devices. (Blanchard Resp. Decl., ¶ 22.) Power MOSFET devices typically have source regions, body regions, an epitaxial layer in which the source and body regions are formed, gate electrodes, and a substrate on which the epitaxial layer is deposited. (*Id.*) The '630 patent relates to a method of making power MOSFET devices having purportedly enhanced ruggedness due to the presence of, among other things, a double implant step to form a "self-aligned shallow high concentration body dopant region" and a "self-

aligned deep high concentration body dopant region." (*Id.*) A representative embodiment from the specification is set forth below:



(Jacobs Resp. Decl., Ex. 10, ('630 patent, Fig. 3C (annotated); Blanchard Resp. Decl., ¶ 22.) The embodiment illustrated above is a power MOSFET including a substrate, an epitaxial layer formed on top of the substrate, and source and body regions formed in the epitaxial layer. (Blanchard Resp. Decl., ¶ 23.) It also includes gate electrodes formed on the surface of the epitaxial layer, as well as shallow and deep high concentration body dopant regions formed in the body region. (*Id.*)

2. "applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates" ('630 patent, claim 1)

Fairchild's Proposed Construction	AOS's Proposed Construction
Applying a mask having a plurality of openings to allow the removal of areas of a polysilicon layer to form a plurality of polysilicon gates corresponding to the plurality of areas of the mask which are not open.	The meaning of this phrase is clear and unambiguous to a person of ordinary skill in the art, and thus it need not be construed by the court.

The '630 patent has one independent claim, which is set forth below (the disputed claim language is in bold):

> 1. A method for fabricating a MOSFET transistor on a substrate comprising steps of:
>
> a) forming an epi-layer of a first conductivity type as a drain region in said substrate and then growing an initial oxide layer over said epi-layer;

> (b) applying an active mask for etching said active layer to define an active area followed by depositing an overlaying polysilicon layer thereon and ***applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates***;
>
> (c) removing said polysilicon mask then carrying out a body implant of a second conductivity type followed by performing a body diffusion for forming a plurality of body regions;
>
> (d) applying a source blocking mask for implanting a plurality of source regions in said body regions with ions of said first conductivity type followed by removing said source blocking mask and a source diffusion process;
>
> (e) forming an overlying insulation layer covering said MOSFET device followed by applying a contact mask to open a plurality of contact openings there-through; and
>
> (f) performing a low energy body-dopant implant and high energy body dopant implant to form a self-aligned shallow high concentration body dopant region and a self-aligned deep high concentration body dopant region.

(Jacobs Resp. Decl., Ex. 7 ('630 patent, col. 9, ln. 58 - col. 10, ln. 19).)

The primary dispute concerning this term is how a polysilicon mask is used in connection with an etching process to "define" polysilicon gates, i.e., the dispute is over what it means for a mask **to "define"** a feature in the device. The claim itself refers to four separate masks used in the claimed process. The first, an "active mask," is used to define the active area, which is the area of the chip in which the active transistor cells are formed (as opposed to the periphery of the chip). The second mask, a "polysilicon mask," is used to define the polysilicon gates that become part of the active transistor cells. The third mask, a "source blocking mask," is used to define the locations of the source implants within each of the active transistor cells. The fourth mask, a "contact mask," is used to define the locations of the contact openings that are positioned between the gates in the active transistor cells. (Blanchard Resp. Decl., ¶ 42.)

The claim requires the deposition of a polysilicon layer. It also requires "applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates." A polysilicon mask is simply a pattern with open and closed areas that is applied to the polysilicon layer. (*Id.* at ¶¶ 48, 49.) When the polysilicon layer is subjected to an etching process, the polysilicon is removed in the exposed areas of the polysilicon corresponding to the open areas of the mask, and

polysilicon remains in the unexposed portions of the polysilicon layer corresponding to areas of the mask that are not open. (*Id.* at ¶ 48.) Accordingly, a person of ordinary skill in the art would understand a polysilicon mask "defines" polysilicon gates when gates are formed which correspond to the areas of the mask which are not open. (*Id.* at ¶¶ 40, 48.)

a) Fairchild's Proposed Construction Is Correct and Supported By The Intrinsic Evidence

Fairchild's construction is supported by the specification, which explains how the four separate masks identified above are each used to define a respective feature of the device. In particular, the specification teaches the one and only way of what it means to "define" polysilicon gates in the polysilicon layer through the use of a mask. It is essentially a three-step process.

First, the specification discloses the formation of a structure which includes a semiconductor substrate, an epitaxial layer deposited on the substrate, and an initial oxide layer formed on the epitaxial layer. (Jacobs Resp. Decl., Ex. 107 ('630 patent, col. 6, ln. 67 - col. 7, ln. 9); Blanchard Resp. Decl., ¶ 43.) The initial oxide layer covers the entire surface of the die. An “active mask” is then used to open up the active area by exposing it to an etch. (*Id.*) The active area is shown to the left of the “initial oxide layer” shown as feature 115 below. If one were to look down on the die from above, the active area would look like a generally square area of exposed epitaxial layer surrounded by the initial oxide layer.

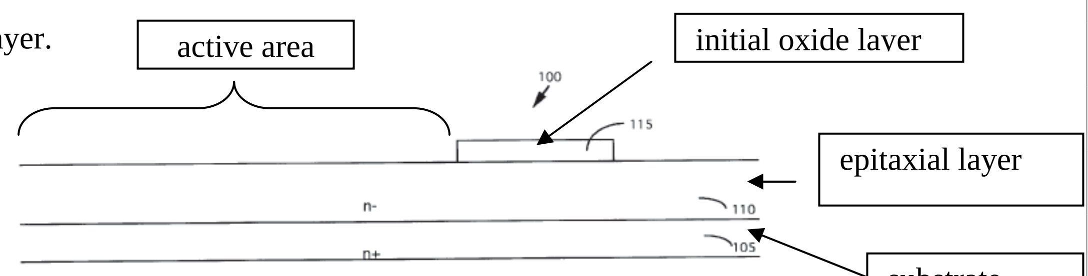


FIG. 5A

(Jacobs Resp. Decl., Ex. 10 ('630 patent, Fig. 5A (annotated)); Blanchard Resp. Decl., ¶ 43.)

Second, a gate oxide layer is then grown on the top surface of the exposed epitaxial layer, and a polysilicon layer is subsequently deposited on the gate oxide layer, thereby covering the top surface with polysilicon:

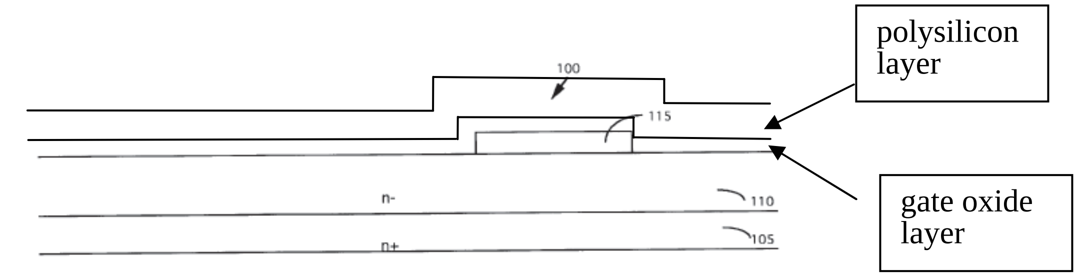


FIG. 5A

(Jacobs Resp. Decl., Ex. 7 ('630 patent, col. 7, lns. 9-12 & Fig. 5A (supplemented to show features described in specification)); Blanchard Resp. Decl., ¶ 44.)

There are no defined gates at this point in the process. After the deposition of the polysilicon layer, a “polysilicon mask” is used to define the polysilicon gates, by etching (removing) portions of the polysilicon layer where the gates will not be present. (Jacobs Resp. Decl., Ex. 7 ('630 patent, col. 7, lns. 14-16); Blanchard Resp. Decl., ¶ 45.) This final step results in the presence of polysilicon gates on the top surface of the substrate, *and the shapes of the polysilicon gates correspond to the shapes of the areas of the mask which are not open to the etching process*:

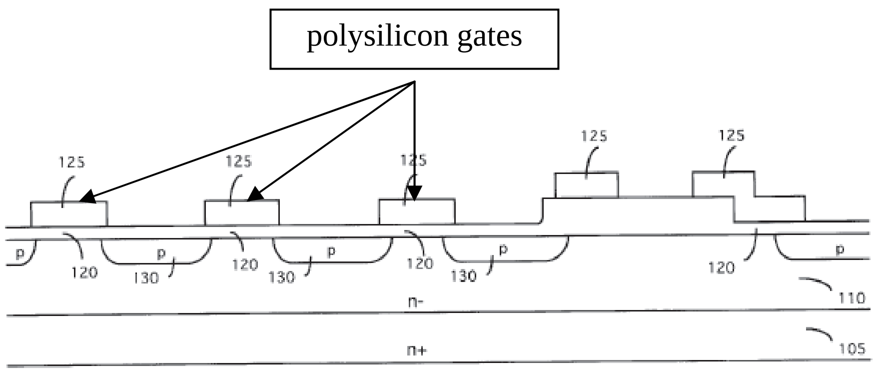


FIG. 5B

(Jacobs Resp. Decl., Ex. 10 ('630 patent, Fig. 5B (annotated)); Blanchard Resp. Decl., ¶ 45.)

Fairchild's proposed construction is consistent with the process in the specification described above. The locations of the gates correspond to the unexposed areas of the polysilicon which are protected by the polysilicon mask. The specification does not disclose or suggest any other way in which polysilicon gates are "defined"[3] in a polysilicon layer through the use of a mask for etching.

[3] In the context of claim 1 of the ‘630 patent, the word “define” itself means “to fix or mark the limits of,” Jacobs Resp. Decl., Ex. 11 (Merriam-Webster’s Collegiate Dictionary, 10th Ed., 1999), at p. 303; “to delineate the outline or form of;” Jacobs Resp. Decl., Ex. 12 (The American Heritage Dictionary, 2nd College Ed., 1985), at p. 375.

(Blanchard Resp. Decl., ¶ 46.) Accordingly, Fairchild's proposed construction is appropriate. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (*en banc*) ("As we stated in *Vitronics*, the specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'").

b) AOS's Arguments Against Construing This Claim Term Should Be Rejected

Although AOS seeks to avoid having the Court construe the term at all, AOS’s opening brief reveals that AOS interprets the claim term in an incorrect way. First, AOS argues the claim term should be interpreted by breaking it into three phrases, and interpreting each phrase individually. (AOS Opening Brief at pp. 14-16.) AOS's approach is incorrect because it removes the claim construction analysis from the appropriate context. The claim requires a relationship between the application of the polysilicon mask and the definition of the polysilicon gates. (Blanchard Resp. Decl., ¶ 47.) Indeed, the three phrases that AOS would treat separately are intentionally linked by the claim language: “applying a polysilicon mask ***for*** etching said polysilicon layer ***to*** define a plurality of polysilicon gates.” (Jacobs Resp. Decl., Ex. 10 ('630 patent, col. 9, lns. 65-67 (emphasis supplied).) Yet, AOS interprets the claim term to require no relationship among the phrases at all, and instead urges that the term simply requires individual steps of "applying," "etching," and "defining" without any connection between them. Under AOS's interpretation, one can practice the claimed invention by (1) applying a polysilicon mask and (2) defining polysilicon gates, *even if the polysilicon mask plays no role at all in defining the gates*. This is inconsistent with the claim language and specification. (Blanchard Resp. Decl., ¶ 47.)

Second, AOS argues Fairchild’s construction is incorrect because it would exclude trenched gate devices. (AOS Opening Brief at pp. 15-17.) In doing so, AOS asserts that the context in which the word "define" should be interpreted depends on the type of device configuration. For planar devices, according to AOS, a gate is defined by its horizontal dimension. For trench devices, AOS contends a gate is defined by its vertical dimension. (*Id*. at p. 15.) There is absolutely no support for this statement. As explained above, the specification provides a straightforward explanation concerning the meaning of "define" in the context of the claimed invention. The specification does

not teach a different method depending on whether the gate is planar or trenched. AOS's contentions are simply attorney argument and are not even supported by its own expert or any other evidence. Indeed, AOS's expert fails to address the critical issue of what it means to *define* the polysilicon gates through the use of a polysilicon mask. (Salama Decl. (Docket No. 148), ¶ 7.) Instead, AOS's expert merely describes the removal of polysilicon without explaining how the areas to be removed are defined by a mask or anything else. (*Id.*)

AOS's entire argument relies on Figure 6 in the specification. (AOS Opening Brief at p. 14.) AOS's description of the figure, however, is *unsupported speculation*. AOS asserts that the figure discloses a trenched gate which is defined in part by the application of a mask that only exposes the polysilicon in the trench, so that the vertical dimension of the gate is defined upon completion of the etching process. (*Id.*) Yet AOS does not provide any support for its characterization of the figure -- it does not cite the specification, testimony from its own expert, or any other evidence.

In addition to being unsupported speculation, AOS's description of the figure is also ***wrong***. A person of ordinary skill in the art would understand that the gates in Figure 6 are made by an entirely different process than the one AOS suggests. (Blanchard Resp. Decl., ¶ 52.) In particular, ***one skilled in the art would understand that a polysilicon mask plays no role whatsoever in defining the trenched gate shown in the figure***. Trenched gates are typically formed by etching the epitaxial layer to form the trenches, depositing a gate oxide layer and a gate material in the trenches and on the surface of the substrate, and then exposing the entire active area, including all the trenches, to an etching process. (*Id.*) A polysilicon mask is not used to only expose the gate when making trenched gates. (*Id.*) The relevant steps of a typical process for making trenched gates are illustrated below.

The first step is the etching of trenches into an underlying epitaxial layer:

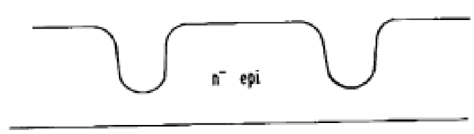


FIG. 4D.

(Blanchard Resp. Decl., ¶ 51.) The next step is the growth of a thin gate oxide layer and a polysilicon layer. The polysilicon layer fills the trenches and also covers the top surface of the device:

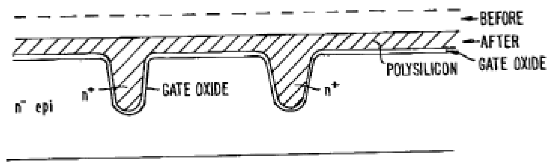


FIG. 4E.

(*Id.*) The next step is the application of a mask to the substrate. The mask exposes the active area as a whole, and thus it does not define the gates in the trenches. It is instead used to define other structures on the surface of the substrate. (*Id.*) After the mask is applied, an etching process is performed to etch away the polysilicon that is situated on the top surface of the active area, leaving polysilicon in the trenches. This results in most of the polysilicon layer on the surface of the substrate being etched away, and some remaining in the trenches:

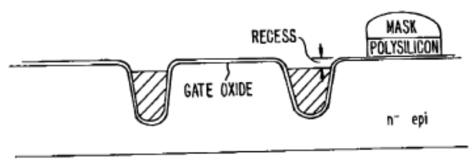


FIG. 4F.

(*Id.*) Consequently, a polysilicon mask plays no role in establishing the shape of the trenched gates. ***In fact, the trenched gates would have the same shape even if no polysilicon mask were used.*** (*Id.*) Accordingly, AOS's argument that a polysilicon mask is used to "define" trenched gates in Figure 6 makes no sense at all.

Finally, AOS argues that, as a matter of law, the claim language must be construed to cover the embodiment shown in Figure 6 on the grounds that a claim allegedly must cover every embodiment disclosed in the specification. (AOS Opening Brief at p. 16.) That is not the law. It is completely appropriate to construe claim language to cover at least one embodiment in the specification, even if other embodiments are not covered. *See, e.g., Sinorgchem Co. Shandong v. ITC*, 511 F.3d 1132, 1138 (Fed. Cir. 2007) (holding that a claim construction is appropriate even though it does not cover one of the embodiments disclosed in the specification). Moreover, the *Vitronics* case AOS cites does not even support its argument. In *Vitronics*, the specification disclosed only one embodiment, and the Federal Circuit rejected a claim construction which did not cover that embodiment. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583-84 (Fed. Cir. 1996). In other words, the Federal Circuit refused to adopt a construction that would not cover ***any*** embodiment disclosed in the specification.

That is plainly not the case here.

The only discussion of a trench MOSFET in the ‘630 patent consists of 20 lines of text found at column 8, ln. 55 to column 9, ln. 7, with a reference to Figure 6. The focus of that discussion is on the use of shallow and deep self-aligned high concentration body implants, which is the crux of the claimed invention. There is no discussion about how to form the gates in the trench device. (Blanchard Resp. Decl., ¶ 53.) Fairchild's proposed construction covers the planar devices disclosed in the specification. Accordingly, it would be incorrect to reject a claim construction which is plainly appropriate on the grounds that it does not cover one, throw-away example of a trench device.

C. The ‘776 Patent

1. Background of the Technology

The ’776 patent is directed to a power MOSFET that has lower threshold voltage and higher resistance to punch-through by using a compensating implant into the body region of the device. Jacobs Resp. Decl., Ex. 13. In a power MOSFET, current can flow between the source and drain regions when a voltage higher than the threshold voltage is applied to the gate. If such a voltage is not applied to the gate, the device generally cannot conduct electricity, except in unwanted circumstances such as breakdown and punch-through. One of the goals in designing power MOSFETs is to reduce the threshold voltage, since doing so reduces the amount of power required to operate the device. (Blanchard Resp Decl., at ¶¶ 19-20.) The threshold voltage cannot be made too low, however, since the device could turn on when it is not intended to. (*Id*. at ¶ 20.) Prior to the ‘776 patent, several techniques were available for reducing threshold voltage. One technique was simply to reduce the length of the conductive channel between the source and drain regions by performing a deeper source implant. (*Id*.) Another way was to modify the doping profile of the body region. (*Id*.) The technique claimed in the ‘776 patent was to reduce the dopant concentration of a portion of the body region near the source/body junction by means of a “compensating” implant.

2. "Compensating" ('776 patent, claim 1)

Fairchild's Proposed Construction	AOS's Proposed Construction
implanting impurities of the second conductivity type into the body region such that the peak concentration of that implant is located in the body region, and such that the conductivity type at the location of the peak concentration of that implant does not change	implanting into the body region material having conductivity type opposite the conductivity type of the body region

Fairchild's proposed construction is consistent with the understanding of a person of ordinary skill in the art and is supported by the '776 patent specification. AOS's proposed construction is entirely unsupported by the specification. Even the extrinsic evidence cited by AOS undermines its proposed construction. Accordingly, Fairchild's proposed construction should be adopted.

a) Fairchild's proposed construction correctly recognizes that an implant is located where its peak concentration occurs

Fairchild's proposed construction reflects the understanding of a person of ordinary skill in the art that a dopant implant is "located" where its peak concentration occurs. A person of ordinary skill in the field of semiconductor power devices understands that when dopant ions are implanted into a substrate, they do not all travel the same depth into the substrate. (Blanchard Resp. Decl., ¶ 32.) Rather, the dopant ions come to rest at different depths into the substrate so as to have a nearly-Gaussian, or bell-shaped, distribution in the vertical direction. (*Id.*) The dopant concentration is highest at the peak of the curve and diminishes with increasing distance from the peak. (*Id.*) A person of ordinary skill in the art would understand that the location of an implant is considered to be the location of the peak concentration of the implant. (*Id.*) Fairchild's proposed construction is consistent with this understanding.

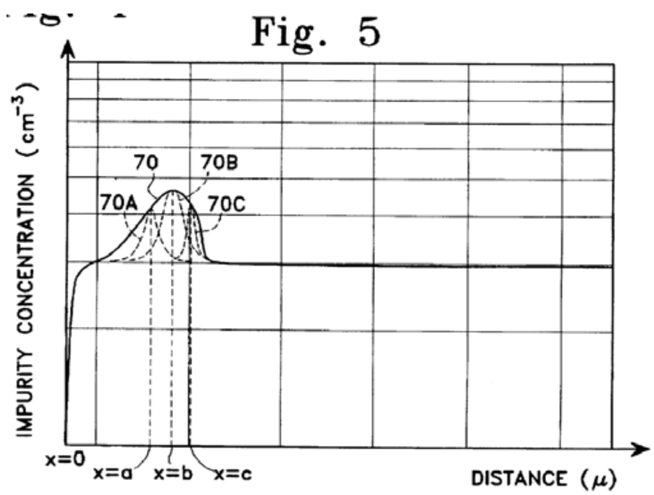
As expected, the '776 patent specification recognizes that an implant is located where its peak concentration occurs. The '776 patent specification repeatedly refers to the "penetration distance" or the "distances from the planar surface" of each of the individual implants that form the compensating implant as being at a specific depth, namely x=a, x=b, and x=c. For example, column 5, lines 50-61 of the patent state that:

> Shown in FIG. 5 is the resultant impurity concentration profile represented by a compensation curve 70 which in essence is a

> superimposition of three individual implantation curves 70A-70C. The ***penetration distances*** of the individual implantation x=a, x=b, and x=c are first determined. The process of ion implantation is employed to place various dosages of dopant into the substrate 34. An exemplary technique for implanting a dopant at a ***predetermined penetration distance*** into a silicon substrate can be found in a publication by Wolf et al., "Silicon Processing for the VLSI Era", Vol. 1, Process Technology, pages 285-291. (Jacobs Resp. Decl., Ex. 14.)

(Emphasis added). Similarly, column 7, lines 39 to 56 of the patent state that the three implants that form the "compensation curve 70" are located at a specific distance from the planar surface, and specify that the distances are x=a, x=b, and x=c.

Figure 5 of the patent shows that the values x=a, x=b, and x=c correspond to the location of the peak concentration of each implant.



Furthermore, the chart shown in Figure 6 and the corresponding text in the patent also make clear that the location of an implant is where its peak concentration occurs and not a range of depths. (See col. 5, ln. 62 to col. 6, ln. 6.) Thus, the patent describes the location of the implants that, in the aggregate, form the compensating implant as being located where the peak concentration of the implant occurs.

b) Fairchild's proposed construction correctly recognizes that the peak concentration of the compensating implant must be in the body region

Figures 4 and 5 and the corresponding text in the specification of the ‘776 patent make clear that the peak of the compensating implant in the preferred embodiment is located in the body region.

The patent states at column 7, lns. 40-52 that:

> The step of body region compensation is the next step in the fabrication process. Reference is now directed back to FIGS. 3-5. To secure a reasonably level body diffusion curve 66 near the body junction $x=x_{js}$, successive implantations at various distances from the planar surface 36 (FIG. 3) are preferred. It this method, boron ions are implanted at distances of x=a, x=b and x=c from the planar surface 36 (FIG. 3), which distances correspond to the individual implant profiles 70A, 70B and 70C, respectively, as shown in FIG. 5. ***Profile 70B*** can be higher in amplitude and can be ***coincident with the peak value of the body diffusion curve 66 had the curve 66 not been compensated (that is, the uncompensated curve 30)***. (Jacobs Resp. Decl., Ex. 13.)

Figure 4 shows that the peak value of the uncompensated curve 30 (shown as a dashed line) is located to the right of the source-body junction, identified as $x=x_{js}$ in Figure 4. Figure 5 shows that the peak value of profile 70B is at the same location as the peak value of the compensation curve 70.

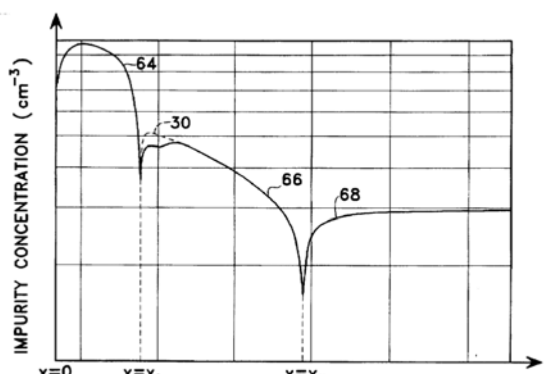
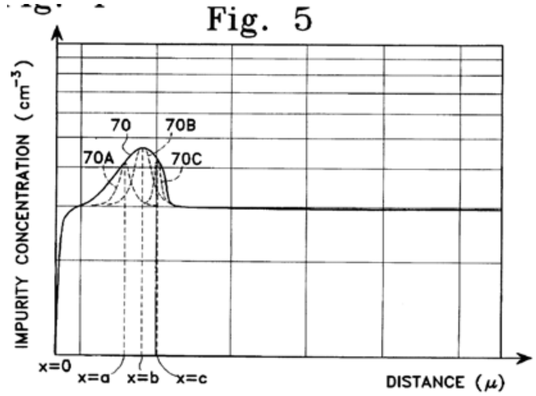


Fig. 4

Fig. 5


Since the peak value of implant profile 70B (and therefore also the peak profile of compensation curve 70) in Figure 5 is at the same location as the peak location of uncompensated curve 30 in Figure 4, it necessarily follows that the peak value of the compensation curve 70 is located *in the body region*, not in the source region. This is consistent with the claim language which states that the compensating implant is made "in said body region." (Blanchard Resp. Decl., at ¶ 36.)

AOS erroneously contends that defining the "compensating" limitation to require peak concentration to be in the body region is contradicted by the '776 patent specification. In support of this argument, AOS cites Figures 4 and 5 of the patent and the corresponding text. In particular, AOS contends that under Fairchild's proposed construction, the implant corresponding to dotted line 70C would be a compensating implant, whereas the implant corresponding to dotted line 70A would not be

a compensating implant. Contrary to AOS's argument, the ‘776 patent never refers to the three implants identified as 70A, 70B and 70C in Figure 5 as being *individual* "compensating implants." Rather, it merely refers to them as "individual implant profiles." It is the *aggregate* dopant profile resulting from the three implants shown in Figure 5 -- *not any one implant taken in isolation* -- that creates the "compensation curve 70" shown in Figure 5. (Blanchard Resp. Decl., at ¶¶ 34-35.)

c) Fairchild's proposed construction correctly recognizes that a compensating implant cannot convert the conductivity of the material being compensated

Fairchild’s proposed construction also properly requires that the compensating implant should reduce the net concentration of dopants at the location of the peak, but that the conductivity type should remain the same. Fairchild’s proposed construction is supported by Figure 4 of the patent, which shows the dopant profile of the source and body regions.

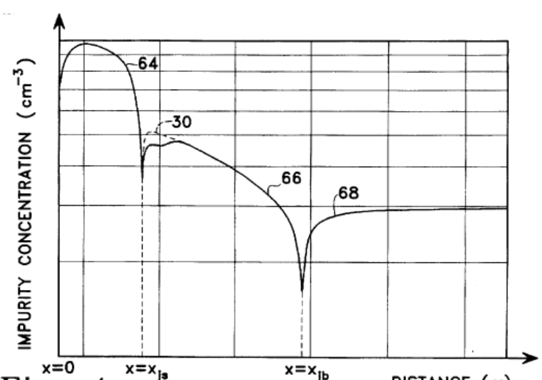
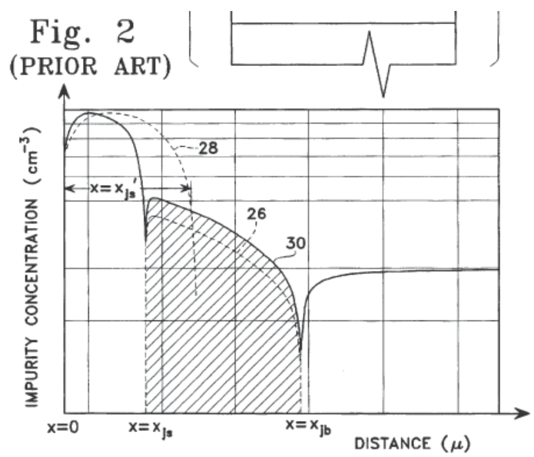


Fig. 4

Figure 4 shows the doping profile of the source region (between x=0 and x=x_{js}), and the doping profile of the body region (between x=x_{js} and x=x_{jb}). The dotted line 30 shows what the doping profile of the body region would look like without the compensating implant, whereas solid line 66 shows the actual doping profile of the body region with the compensating implant. The dip in line 66 to the right of x=xjs, underneath dotted line 30, shows that the compensating implant has caused the net dopant concentration to decrease in the body region (alongside the source region), *but that the conductivity type remains the same*. If the conductivity type were reversed by the compensating implant, there would not be a dip in curve 66. Rather, the body/source junction located at x=xjs would simply move to the right. This is because such an implant would not be a compensating implant, but rather would be another source implant. (Blanchard Resp. Decl., at ¶ 36.)

There is no support in the ‘776 patent specification suggesting that a “compensating” implant can convert the conductivity type. Such an implant would simply result in a deeper source region and therefore also a shorter channel region between the source and the drain. (Blanchard Resp. Decl., ¶ 37.) The patent specification teaches away from techniques that shorten the channel region. ('776 patent at col. 3, lns. 23-31.) In particular, the background section of the patent states that a prior art technique for reducing threshold voltage was to diffuse the source region deeper into the device. (*Id.*) This would have the effect of moving the source-body junction deeper into the device, as is shown in Figure 2.



The patent states that this deepening of the source-body junction results in the same depletion layer encroachment problem as other prior art techniques because the depletion region has a shorter distance to travel to reach punch-through. ('776 patent at col. 3, lns. 28-31.) The effect of diffusing the source region deeper into the device is the same as the effect of performing an implant having a peak concentration in the source region (as opposed to body region) -- they both push the source-body junction ($x=x_{js}$) deeper into the device. (Blanchard Resp. Decl., ¶ 37.) In view of this discussion of the prior art, a person of ordinary skill in the art would **not** read the ‘776 patent claims as covering an implant having a peak dopant concentration in the source region. (*Id.*)

AOS argues that a compensating implant can convert the conductivity type of the material into which the dopants are implanted. None of the extrinsic evidence cited by AOS, however, supports this proposition. The IEEE dictionary cited by AOS defines "doping compensation" as "[a]ddition of

donor impurities to a p-type semiconductor or of acceptor impurities to an n-type semiconductor." (Jacobs Resp. Decl., Ex. 15.) This definition says nothing about converting the conductivity of the semiconductor from one type to another, and therefore cannot be read as supporting AOS's proposed construction. The Wiley Electrical and Electronics Engineering Dictionary (2004) defines "compensated semiconductor" as "[a] semiconductor with two types of impurities or imperfections, in which the electrical effects of one type of impurity or imperfections ***partially cancel*** the other. For instance, a donor impurity ***partly annulling*** the electrical effects of an acceptor impurity." (Emphasis added). (Jacobs Resp. Decl., Ex. 13.) The language "partially cancel" and "partially annul" actually refutes AOS's proposed construction and support Fairchild's. If the compensating implant could convert the conductivity of the semiconductor from one type to another, the definition would say "completely cancel" or "completely annulling" or some similar language. Even the declaration of Dr. Salama supports Fairchild's proposed construction by stating that "[w]hen a semiconductor region is compensated, the introduced dopants ***partially cancel*** the pre-existing dopants of the opposite conductivity type." (Emphasis added). AOS has provided no evidence whatsoever in support of its assertion that a compensating implant can convert the conductivity type of the semiconductor material.

III. CONCLUSION

Fairchild respectfully submits that its proposed constructions are supported by the claims, the patent specifications and the prosecution histories of the AOS patents. In addition, as explained by Dr. Blanchard, Fairchild's constructions are consistent with the understanding of a person of ordinary skill in the art. AOS's proposed constructions, however, find no support in the intrinsic evidence and are incorrect from a technical perspective. For the reasons given and under the authorities cited, Fairchild respectfully requests that the Court adopt Fairchild's proposed constructions.

DATED: March 27, 2008

Respectfully submitted,

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